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LIST C	F P	U.S. DEPARTMENT OF CONCESS. PATENT AND TRADESORY SPYTCE RIOR ART APPLICANT ROV. 18 2005	Atty. Docket No. FIS920030221US1 Applicants Cheng, et al.	Serial No. 10/605,227
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T- ****		Kern Rim, et al., "Characteristic: PMOSFETS". 2002 Symposium on VLS	s and Device Design of Sub I Technology Digest of Tec	-100 nm Strained Si N- and hnical Papers, IEEE, pp. 98-99.
		Gregory Scott, et al., "NMOS Drive Isolation Induced Stress". Intern		by Transistor Layout and Trench Meeting, 34.4.1, IEEE, September 1999
		F. Ootsuka, et al., "A Highly Dense System-on-a-Chip Application". In	e, High-Performance 130nm ternational Electron Devic	Node CMOS Technology for Large Scale es Meeting, 23.5.1, IEEE, April 2000.
		Shinya Ito, et al., "Mechanical Str Submicron Transistor Design." Inte		itride and its Impact on Deep s Meeting, 10.7.1, IEEE, April 2000.
		A. Shimzu, et al., "Local Mechanica Enhancement". International Electr	al-Stress Control (LMC): A ron Devices Meeting, IEEE,	New Technique for CMOS-Performance March 2001.
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		C.J. Huang, et al., "Temperature Dep Effects in Bipolar Transistors". IEE	endence and Post-Stress R E 1991 Bipolar Circuits a	ecovery of Hot Electron Degradation dd Technology Meeting 7.5, pp. 170-73
		S.R. Sheng, et al., "Degradation and Stressing". Pp. 14-15.	Recovery of SiGe HBTs Fo	Towing Radiation and Hot-Carrier
		Z. Yang, et al., "Avalanche Current Heterojunction Bipolar Transistors".	Induced Hot Carrier Degrad	lation in 200 GHz SiGe

07/07/2006 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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KR		H.S. Momose, et a in Bipolar Transi June 1994, pp. 97	stor for Bi-CMOS"	the Temperature De	ependence of Hot-Ca ons on Electron Dev	rrier-Induced Degradation ices, vol. 41, no. 6,
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KR.		4,958,213	9-18-90	Eklund	, et al.	25	378		
		5,006,913	4-9-91	Sugaha	ra, et al.	25			
		5,060,030	10-22-91	Hoke, e	et al.	25	1 194		
		5,081,513	1-14-92	Jackson	o, et al.	25	57		
KR		5,108,843	4-28-92	Ohtaka	, et al.	428	446		
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KR		US 2002/0086497 A1	7-4-02	Kwok		438	424		
		US 2002/0090791 A1	7-11-02	Doyle,	et al.	438	.396		
		US 2003/0032261 A1	2-13-03	Yeh, et	aL	438	451		
KR		US 2003/0040158 A1	2-27-03	Saitoh		438	279		
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		Gregory Scott, et al., "N International Electron D	MOS Drive Cur evices Meeting,	rent Redu 34.4.1, IE	ection Caused by Transiston EE, September 1999.	r Layout ai	d Trench Isolatio	on Induced Stress	
		P. Ootsuka, et al., "A Hi Application." Internation	ghly Dense, High mai Electron De	n-Perform vices Mee	nance 130nm Node CMOS* ting, 23.5.1, IEEE, April 20	l'echnology 100.	for Large Scale	System-on-a-Chlp	
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		4,665,415	5-12-87	Esaki,	et aL	7257	190	
		4,853,076	8-1-89	Tsaur,	et al.	438	479	
		4,855,245	8-8-89	Neppl,	et al.	437	8 207	
KR	<u> </u>	4,952,524	8-28-90	Lee, et	al.	438	3437	
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VR		US 2001/0009784 A1	7-26-01	Ma, et	al.	438	197	
		US 2002/0063292 A1	5-30-02	Armstı	rong, et al.	25	1 367	
		US 2002/0074598 A1	6-20-02	Doyle,	et al.	257	345	
VR		US 2002/0086472	7-4-02	Roberd	ls, et al.	438	197	
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		Kern Rim, et al., "Tre Devices Meeting, 26, 8	insconductance En I, 1, IEEE, Septem	hanceme ber 1998.	at in Deep Submicron St	rained-Si n-M	OSFETs". Inter	national Electron
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		Kern Rim, et al., "Ch VLSI Technology Dig	aracteristics and Dest of Technical Pa	evice Des	lgn of Sub-100 nm Strai E, pp. 98-99.	ned SI N- and	PMOSFETs." 2	002 Symposium o
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		5,310,446	5-10- 94	Konish	i, et aL	117		58		
		5,354,695	10-11-94	Leedy		438	3_	411		
		5,371,399	12-6-94	Burroughes, et al.		25	7	451		
KR		5,391,510	2-21-95	Hsu, et	al.	43	8	301		
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KR US 2003/0057184 A1			3-27-03	Yu, et	al.	all	p	79		
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		5,471,948	12-5-95	Burrou	ghes, et al.	438	93	
		5,557,122	9-17-96	Shrivas	tava, et al.	25	309	
		5,561,302	10-1- 96	Candelaria		25	1 24	
KR		5,565,697	10-15-96	Asakaw	/a, et al.	25	347	
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	\dashv	G. Zhang, et al., "A New IEEE Transactions on E	'Mixed-Mode' lectron Devices,	Reliability vol. 49, po	Degradation Mechanism io. 12, December 2002, pp. 2	Advanced 151-56.	Si and SiGe Big	olar Transistors.
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		5,592,007	1-7-97	Leedy		257	347			
		5,592,018	1-7-97	Leedy		257	619			
		5,670,798	9-23-97	Schetzina		25	1 96			
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		C.J. Huang, et al., "Ten Transistors." IEEE 199	nperature Depon 1 Bipolar Circu	dence and its and Te	Post-Stress Recovery of H chnology Meeting 7.5, pp.	ot Electron 170–173.	Degradation Ef	ects in bipolar		
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KR		5,683,934	11-4-97	Candel	aria	438			
		5,840,593	11-24-98	Leedy		438	6 6		
		5,861,651	1-19-99	Brasen,	et al.	25	1 411		
		5,880,040	3-9-99	Sun, et al.			3 769		
KR		5,940,716	8-17 -99	Jln, et s	վ.	438	424		
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		5,946,559	8-31-99	Leedy			438	157		
		5,960,297	9-28-99	Saki			438	424		
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		6,046,464	4-4-00	Schetzi	na	257	96		
		6,066,545	5-23-00	Doshi,	et al.	438			
		6,090,684	7-18-00	Ishitsul	ka, et al.	439	3 424		
KR		6,107,143	8-22-00	Park, e	t al.	438	296		
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		6,221,735	4-24-01	Manley	, et al.	438			
KR		6,228,694	5-8-01	Doyle,	et al.	438	199		
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		6,265,317	7-24-01	Chiu, e	t aL		+38	711	- 	
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KR		6,281,532			8-28-01	Doyle, et al.		2	257 2		88				
		6,28	4,623			9-4-01	Zhang, et al.				438 424		24		
		6,28	4,626			9-4-01	Kim			13	738 433		33	3	
	6,319,794			11-20-01	Akatsu	ı, et aL		4:	38	4	24				
KR		6,36	1,885			3-26-02	Chou			4	128	100	690		
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				U.S	PATENT	DOCUMENTS					
*EXAMINER INITIAL	HEP	DOCUMENT	NUMBER	DATE		NAMB	CLASS	8UBCLASS	PILING DATE		
KR		6,362,082		3-26-02	Doyle, e	et al.	438	523			
		6,368,931		4-9-02	Kuhn,	et al.	438	359			
		6,403,486		6-11-02	Lou		439	8 694			
		6,403,975		6-11-02	Brunne	r, et al.	25	7 15	 		
KR		6,406,973		6-18-02	Lee		438	416			
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K	R		6,461,936	10-8-02	von Eb	renwall	438	424		
			6,476,462	11-5-02	Shimiz	ru, et al.	25		, .	
			6,483,171	11-19-02	Forbes	, et al.	125	1 627		
1			6,493,497	12-10-02	Ramda	nni, et al.	385	131		· ——
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1		6,506,652	1-14-03	Jan, et	al.	438	303			
		6,509,618	1-21-03	Jan, et	RL .	25	413			
		6,521,964	2-18-03	Jan, et	al.	ର୍ଚ୍ଚ	413			
KR		6,531,369	3-11-03	Ozkan,	et al.	438	312			
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KR		6,531,740	3-11-03	Bosco,	et al.	25						
		6,621,392	9-16-03	Volant,	et al.	335	78					
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